CLAIM LISTING

Amendments to the claims are reflected in the following listing, which replaces any and all prior versions and listings of claims in the present application:

1. (Currently Amended) A memory controller for controlling a transfer of a datum from a data source to a data destination, comprising:

a delay circuit configured to generate a plurality of delay clock signals at different times, wherein the plurality of clock signals comprises:

a delay clock signal generated at one of shortly after a nominal leading edge and shortly before a nominal trailing edge a data valid window (DVW) of a timing signal, and

a delay signal generated at a nominal midpoint of the DVW;

a plurality of latches responsive to the plurality of delay clock signals, wherein each latch receives a timing signal from the data source and generates a latched signal corresponding to the timing signal received from the data source in response to the delay clock signal; and

a compare circuit responsive to a plurality of the latched signals from the plurality of latches, wherein the compare circuit is configured to generate a comparison signal corresponding to a difference between the plurality of the latched signals.

2. (Canceled)

3. (Currently Amended) A memory controller according to claim ~~2~~1, wherein the compare circuit is configured to generate the comparison signal according to a difference between a latched signal corresponding to the one of the delay signal generated shortly after the nominal leading edge and the delay signal generated shortly before the nominal trailing edge, and a latched signal corresponding to the delay signal generated at the nominal midpoint.

4. (Original) A memory controller according to claim 1, wherein the delay circuit is responsive to the comparison signal and adjusts the timing of at least one of the delay clock signals according to the comparison signal.

5. (Original) A memory controller according to claim 1, wherein the data source exhibits at least one of a voltage time constant and a thermal time constant, and the delay circuit

is configured to generate the delay clock signals at intervals substantially equal to or less than the at least one of the voltage time constant and the thermal time constant.

6. (Original) A memory controller according to claim 1, wherein the delay circuit comprises a multi-tap delay line.

7. (Original) A memory controller according to claim 1, wherein the delay circuit is configured to generate the plurality of delay clock signals in conjunction with a free-running clock signal.

8. (Currently Amended) An electronic system, comprising:

a data source configured to generate a data signal and a timing signal;

a data destination;

means for analyzing the timing signal from the data source, wherein the timing signal analyzing means identifies a data valid window (DVW) in the data signal according to the timing signal;

means for capturing data in the DVW in the data signal from the data source, wherein the data capturing means is configured to generate a delay clock signal at one of shortly after a nominal leading edge of the DVW and shortly before a nominal trailing edge of the DVW, and generate a delay signal at a nominal midpoint of the DVW;

means for transferring the captured data to the data destination; and

means for adjusting the data capturing means according to the timing signal analyzing means.

9. (Currently Amended) A electronic system according to claim 8, wherein the data capturing means comprises a delay circuit configured to generate the delay clock signals, ~~for a nominal edge and a nominal midpoint of a DVW in the timing signal~~.

10. (Currently Amended) A electronic system according to claim 9, wherein the timing signal analyzing means comprises a compare circuit configured to generate a comparison signal according to a difference between a latched signal corresponding to the delay signal generated at one of shortly after the nominal leading edge and shortly before the nominal trailing

edge, and a latched signal corresponding to the delay clock signal generated at the nominal midpoint.

11. (Original) A electronic system according to claim 9, wherein the delay circuit comprises a multi-tap delay line.

12. (Currently Amended) A electronic system according to claim 9, wherein the delay circuit is configured to generate the ~~plurality of~~ delay clock signals in conjunction with a free-running clock signal.

13. (Currently Amended) A data transfer system for transferring data from a data source to a data destination, comprising:

a sampler configured to sample a timing signal from the data source at a plurality of times, wherein the plurality of times comprises a time shortly after a nominal leading edge of a data valid window (DVW) in the timing signal, a time shortly before a nominal trailing edge of the DVW, and at a nominal midpoint of the DVW; and

a compare circuit configured to analyze the samples from the sampler to identify ~~a~~ the leading edge, ~~a~~ the trailing edge, and ~~a~~ the midpoint of ~~a data valid window (DVW) in the timing signal~~ the DVW.

14. (Original) A data transfer system according to claim 13, wherein the compare circuit is further configured to adjust the plurality of times at which the sampler is configured to sample the timing signal.

15. (Original) A data transfer system according to claim 13, wherein the compare circuit is further configured to adjust at least one of the plurality of times at which the sampler is configured to sample the data signal to correspond to at least one of the identified leading edge, trailing edge, and midpoint of the DVW.

16. (Currently Amended) A data transfer system according to claim 13, wherein:

~~the sampler is configured to sample the timing signal at a nominal leading edge, a nominal trailing edge, and a nominal midpoint of the DVW; and~~

the compare circuit is configured to compare the samples from shortly after the

nominal leading edge and shortly before the nominal trailing edge to the sample from the nominal midpoint.

17. (Original) A data transfer system according to claim 13, wherein the sampler comprises a multi-tap delay line.

18. (Original) A data transfer system according to claim 13, wherein the sampler is configured to sample a timing signal from the data source at a plurality of times in conjunction with a free-running clock signal.

19. (Currently Amended) A memory control system for controlling access to a memory module, comprising:

a sampling circuit for taking samples from a timing signal, wherein the samples comprise at least one of a sample from a time shortly after a nominal leading edge of a data valid window (DVW) in the timing signal and a sample from a time shortly before a nominal trailing edge of the DVW, and a sample at a nominal midpoint of the DVW; and

an analysis circuit for receiving the samples from the sampling circuit and identifying ~~a data valid window (DVW)~~ the DVW according to the timing signal.

20. (Original) A memory control system according to claim 19, wherein the sampling circuit generates a data capture signal at the approximate midpoint of the DVW.

21. (Original) A memory control system according to claim 19, wherein the analysis circuit is configured to adjust the samples taken by the sampling circuit to take a midpoint sample at an approximate midpoint from the DVW.

22. (Currently Amended) A memory control system according to claim 19, wherein ~~the sampling circuit takes samples from a nominal midpoint and at least one of a nominal leading edge and a nominal trailing edge of the DVW, and~~ the analysis circuit compares the nominal midpoint sample to ~~the and~~ the at least one of a the sample from a time shortly after the nominal leading edge and the sample from a time shortly before the ~~a~~ nominal trailing edge ~~sample~~.

23. (Original) A memory control system according to claim 19, wherein the analysis circuit comprises a multi-tap delay line.

24. (Original) A memory control system according to claim 19, wherein the sampling circuit takes the samples in conjunction with a free-running clock signal.

25. (Currently Amended) A memory controller for controlling transfers of data from a data source to a data destination, comprising:

a timing circuit for generating a plurality of capture signals, wherein the timing circuit identifies at least one of a leading edge and a trailing edge of a data valid window (DVW) of a timing signal by generating one of a first capture shortly after a nominal leading edge of the DVW and a second capture signal shortly before a nominal trailing edge, and generating a third capture signal at a nominal midpoint.

26. (Currently Amended) A memory controller according to claim 25, further comprising an analysis circuit, wherein the analysis circuit is configured to adjust the timing of the capture signals generated by the timing circuit according to at least one of the identified leading edge and identified trailing edge of the DVW.

27. (Currently Amended) A memory controller according to claim 26, wherein the analysis circuit is configured to selectably adjust the timing of the capture signals generated by the timing circuit according to at least one of a voltage time constant and a thermal time constant associated with the data source.

28. (Currently Amended) A memory controller according to claim 25, further comprising a free-running clock circuit configured to generate a clock signal, wherein the timing circuit generates the capture signals in conjunction with the clock signal.

29. (Currently Amended) A memory controller according to claim 25 wherein the timing circuit generates the capture signals at a nominal midpoint of the DVW.

30. (Original) A memory controller according to claim 25, wherein the timing circuit comprises a multi-tap delay line.

31. (Currently Amended) A method of transferring data from a data source to a data destination, comprising:

sampling a signal to identify at least one of an approximate leading edge and an approximate trailing edge of a data valid window (DVW) by sampling the signal at one of shortly after a nominal leading edge and shortly before a nominal trailing edge; and

adjusting at least one of a the nominal leading edge and a the nominal trailing edge of the DVW according to at least one of the identified approximate leading edge of the DVW and the identified approximate trailing edge of the DVW.

32. (Original) A method of transferring data according to claim 31, further comprising capturing data at an approximate midpoint of the DVW.

33. (Currently Amended) A method of transferring data according to claim 31, further comprising:

sampling the signal at a nominal midpoint; and

comparing a sample from ~~an approximate~~ the nominal midpoint of the DVW to a the sample from at least one of shortly after the nominal leading edge and shortly before the nominal trailing edge of the DVW.

34. (Currently Amended) A method of transferring data from a data source to a data destination, comprising:

sampling a timing signal from the data source at one of shortly after a nominal leading edge of the DVW and shortly before a nominal trailing edge of the DVW;

identifying ~~a data valid window (DVW)~~ the DVW in a data signal according to the sampled timing signal; and

capturing the data in the identified DVW.

35. (Canceled)

36. (Currently Amended) A method of transferring data according to claim ~~35~~34, wherein identifying the DVW further comprises sampling at a nominal midpoint of the DVW in the timing signal and comparing the nominal midpoint sample to one of the shortly after the nominal leading edge sample and the shortly before the nominal trailing edge sample.

37. (Original) A method of transferring data according to claim 34, wherein capturing the data comprises capturing data at an approximate midpoint of the identified DVW.

38. (Original) A method of transferring data according to claim 34, further comprising adjusting the sampling of the timing signal according to the identified DVW in the data signal.

39. (Currently Amended) A method of reading data from a memory, comprising:

requesting a timing signal from the memory;

sampling the requested timing signal at one of shortly after a nominal leading edge of a data valid window (DVW) in the requested timing signal and shortly before a nominal trailing edge of the DVW;

identifying at least one of a leading edge and a trailing edge of the DVW ~~a data valid window (DVW) in the timing signal~~;

calculating an approximate midpoint of the DVW based on the at least one of the leading edge and the trailing edge;

receiving a data signal from the memory; and

capturing a datum from the data signal at an approximate midpoint of a DVW of the data signal corresponding to the approximate midpoint of the DVW of the timing signal.

40. (Canceled)

41. (Currently Amended) A method of reading data according to claim ~~40~~39, comprising comparing the nominal midpoint sample to the at least one of the shortly after the nominal leading edge sample and the shortly before the nominal trailing edge sample.

42. (Currently Amended) A method of reading data according to claim 39, comprising adjusting the sampling of the timing sample according to the identified at least one of the leading edge and the trailing edge of the DVW ~~data valid window (DVW) in the timing signal~~.